REFERENCES

[1] J. Lin and T. Itoh, "Active integrated antennas," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 2186–2193, Dec. 1994.

[2] T. Itoh, "Quasioptical microwave circuits for wireless applications," *Microwave J.*, vol. 38, no. 1, pp. 64–85, Jan. 1995.

[3] J.-F. Luy and P. Russer, *Silicon-Based Millimeter-Wave Devices.* Berlin, Germany: Springer-Verlag, 1994.

[4] M. J. Kelly, J. A. C. Stewart, and A. D. Patterson, "HBT active antenna as a self-oscillating Doppler sensor," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Denver, CO, June 18–13, 1997, pp. 1065–1068.

[5] J. Birkeland and T. Itoh, "Planar FET oscillators using periodic microstrip patch antennas," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1232–1236, Aug. 1989.

[6] M. Schwab, "Determination of the steady state of an oscillator by a combined time-frequency method," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1391–1402, Aug. 1991.

[7] M. O. Thieme and E. M. Biebl, "A fast and rigorous synthesis procedure for (monolithic) millimeter-wave integrated circuit layout," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Denver, CO, June 8–13, 1997, pp. 1009–1012.

[8] G. Gonzalez, *Microwave Transistor Amplifiers.* Englewood Cliffs, NJ, Prentice-Hall, 1984.

[9] A. S. Khanna, "Parallel feedback FETDRO design using 3-port S-parameters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, San Francisco, CA, June 1984, pp. 181–183.

[10] I. J. Bahl and P. Bhartia, *Microwave Solid State Circuit Design.* New York: Wiley, 1988.

[11] A. S. Khanna, "Three-port S-parameters ease GaAs FET designing," *Microwave RF*, vol. 24, no. 12, pp. 81–84, Nov. 1985.

Nonlinear Modeling and Design of Bipolar Transistors Ultra-Low Phase-Noise Dielectric-Resonator Oscillators

M. Regis, O. Llopis, and J. Graffeuil

***Abstract*— This paper presents a design methodology for low phase-noise dielectric-resonator oscillators (DRO's) with applications examples at 4 GHz. Different oscillators topologies are investigated and, finally, three oscillators' configurations have been simulated, realized in discrete elements, and characterized. The best measured phase-noise magnitude is −133 dBc/Hz at 10-kHz offset frequency.**

I. INTRODUCTION

Precise frequency generation is an essential function in telecommunications or radars applications. The phase-noise modeling in microwave free-running oscillators has been a subject of research for many years, but many problems remain unsolved and make the nonlinear design approach very difficult [1]–[5]. However, because of the availability of efficient commercial nonlinear software, it would be in appropriate to base the design of low phase-noise dielectric-resonator oscillators (DRO's) only on the classical small-signal approach [6].

The aim of this paper is to demonstrate that the nonlinear simulation, in spite of being able to predict in all cases the exact phase-noise level of the oscillator, is still a good tool to check if a circuit topology is appropriate for a low phase-noise design. As an example, problems of impedance matching and resonator decoupling are discussed for parallel-feedback oscillators and compared to empirical rules often used by engineers in that field.

Since in this paper our main interest is on ultra-low phase-noise DRO's, only silicon bipolar junction transistors (BJT's) oscillators are investigated. The selected devices feature very good performances in terms of low-frequency (LF) noise, which are still unreached by heterojunction bipolar transistors (HBT's) technology. We found that only some carefully selected devices in the Si/SiGe HBT family could reach these noise levels, with the advantage of higher gain and cutoff frequency compared to the BJT. This study is actually a preliminary study for the design of ultra-low phase-noise Si/SiGe HBT oscillators, but the first results obtained with these devices will be published elsewhere [7]. In this paper, we will focus on oscillator design and topology.

The paper is organized as follows. Section II describes the circuit elements and operating conditions. In Section III, we propose a phase-noise-simulation approach based on input LF, the phase-noise measurements' results obtained on the different oscillators. Finally, these results are compared to the simulation results of Section IV.

II. CIRCUITS ELEMENTS AND OPERATING CONDITIONS

Various high-frequency BJT devices are commercially available, but they all feature different LF noise characteristics. A preliminary test is necessary before choosing a device for a low phase-noise-oscillator application. This can be done either by measuring the LF noise on the quiescent (or nonoscillating) device or by measuring the amplifier-device residual phase noise or directly by measuring the phase noise of test oscillators in which the device is embedded [8]. None of these methods is totally rigorous, but the three give valuable information and almost always converge to the same device classification. The Hewlett-Packard Si-BJT AT41400 has thus been selected. It features an extremely low input voltage noise level of about 0.4 nV/$\sqrt{}$ Hz at 1 kHz (see Fig. 1, curve 2) compared with other devices of the same type [9] and is easily able to sustain a 4-GHz oscillation. The bias conditions are approximately $I_c = 30$ mA and $V_{ce} = 4$ V (see Section III).

The passive part of the oscillator is realized with a Murata's U dielectric resonator featuring an unloaded Q-factor (Q_o) of 8000. This dielectric resonator is supported by a Teflon rod and used in transmission or in reflection modes. In the transmission configuration, it is placed in a metallic housing (copper) and the coupling adjustment is done by magnetic probes. In the reflection configuration, the dielectric resonator is placed near a 50-Ω microstrip line on an alumina substrate.

III. PHASE-NOISE-SIMULATION METHOD

In microwave oscillators, the phase noise is generally attributed to the active device LF noise. This LF noise is converted into frequency fluctuations by a nonlinear mixing process. The classical modeling method uses two noise sources (current and voltage) referred to the transistor input [2], [9]–[12]. The LF noise is measured on the nonoscillating device, and the phase-noise calculation is performed either by using a conversion matrix method, which consists of studying a low-level phase-modulation processor or by using a pushing-factor approach.

The pushing-factor approach is based on the assumption that the device LF equivalent circuit is almost constant in the LF noise

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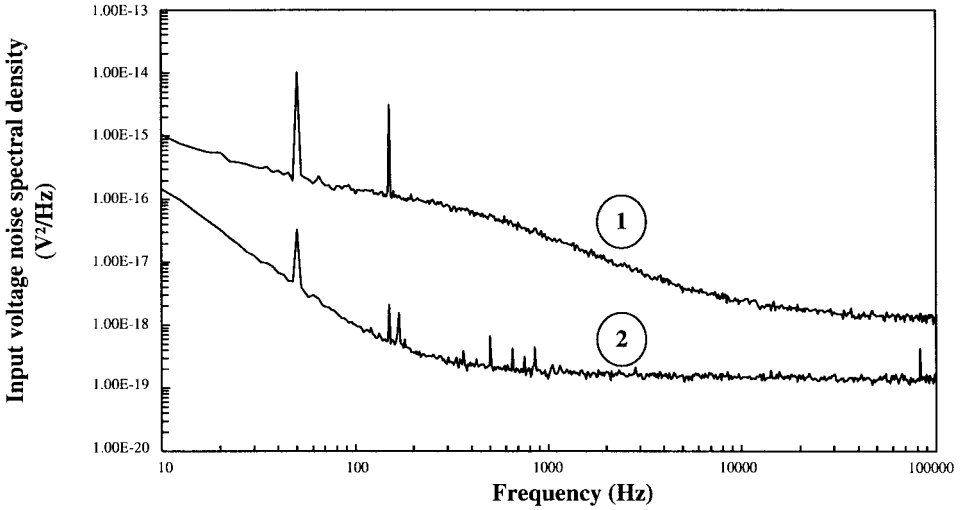

Fig. 1. Equivalent input LF-voltage-noise spectral density. ①: transistor oscillating. ②: transistor at rest ($I_c = 16$ mA, $V_{ce} = 4$ V).

frequency range and suggest that the frequency sensitivity to the noise can be calculated by small dc variations near the nonlinear operating point. It is a two-step procedure, which involves the calculation of the total noise applied to a control voltage in a first step and the frequency sensitivity to this control voltage in a second step. Choosing the external base–emitter voltage as the control voltage, we first calculate the noise ΔV referred to this access and then find the pushing factor as

$$k_p = \frac{\Delta f}{\Delta V_{be_{\mathrm{DC}}}} \ \text{Hz/V}. \tag{1}$$

The single sideband (SSB) phase noise is given by

$$L(f) = 20\log\left(\frac{k_p \Delta V}{\sqrt{2}\cdot f}\right) \ \text{dBc/Hz} \tag{2}$$

where f is the offset frequency and ΔV is the input voltage noise (V/$\sqrt{\ }$ Hz).

In the case of bipolar transistors, either BJT or HBT devices, it is always possible to reduce the influence of one of the two input noise sources, current or voltage. A high LF impedance on the base access ("high" meaning high enough compared to the transistor input LF dynamic impedance) will enhance the noise current effect and cancel the noise voltage effect. On the contrary, a low LF impedancewill enhance the noise voltage effect and reduce the noise current effect. This last configuration is difficult to obtain because the bipolar transistor is a current-controlled device. However, it is always possible to use a high-value capacitance on the base to ensure a low impedance at the noise frequencies while maintaining a high impedance value at dc. It has been shown that, in many cases, the influence on the FM noise of the base current noise is larger than the influence of the voltage noise [11], [12]. Therefore, this high-value capacitance on the base is systematically used in our bipolar oscillators, and only the input voltage noise is considered and measured. This noise is plotted in Fig. 1 for an AT41400 device, the lower spectra corresponding to the quiescent device and the other to the device embedded into a parallel-feedback oscillator. There is a strong difference between the noise sources or, more exactly, the equivalent-input noise sources, when the transistor does and does not oscillate. The problem has been described for FET oscillators [3] and is related to the self-biasing and gain (or other transfer parameters) compression in the nonlinear regime. In this case, both the noise amplitude and shape are modified, including the $1/f$ component of noise. This phenomenon will always occur on transistor models involving extrinsic noise sources. However, an intrinsic noise model for BJT devices that could take into account these self-biasing phenomena has not yet been published. Also note that, in the past, good results have been obtained with the extrinsic noise-source approach [5], [13]. Therefore, with regard to these limitations, it is not possible to calculate the exact oscillator phase noise, but it should be possible to find an oscillator topology featuring a good phase-noise performance.

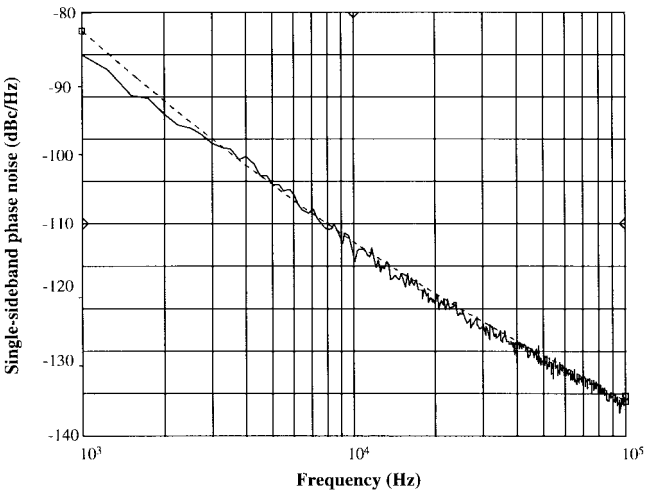

Fig. 2. Simulated and measured phase noise for a parallel-feedback 4-GHz oscillator using a low Q-factor resonator ($Q_L = 160$).

The noise source that will be further considered is the noise source measured under oscillation. As its level is dependent mainly on the compression level of the device under oscillation, the following study will be performed approximately at the same compression level, i.e., close to the 1-dB compression point. It has indeed been found that the low compression-level condition was an interesting condition for a low conversion of the LF noise into phase noise in these oscillators. In most of our calculations, the phase noise is optimum when the losses in the feedback loop are close to the transistor gain.

Other parameters that can have a strong effect on phase noise are the dc bias point and the LF feedback elements. As shown in [11]–[13] a high enough collector-current bias point must be chosen to minimize the noise-conversion process. Also, an active LF feedback may be used to cancel the input noise-source effect [13], but this often results at microwaves frequencies in transistor instabilities. Increasing

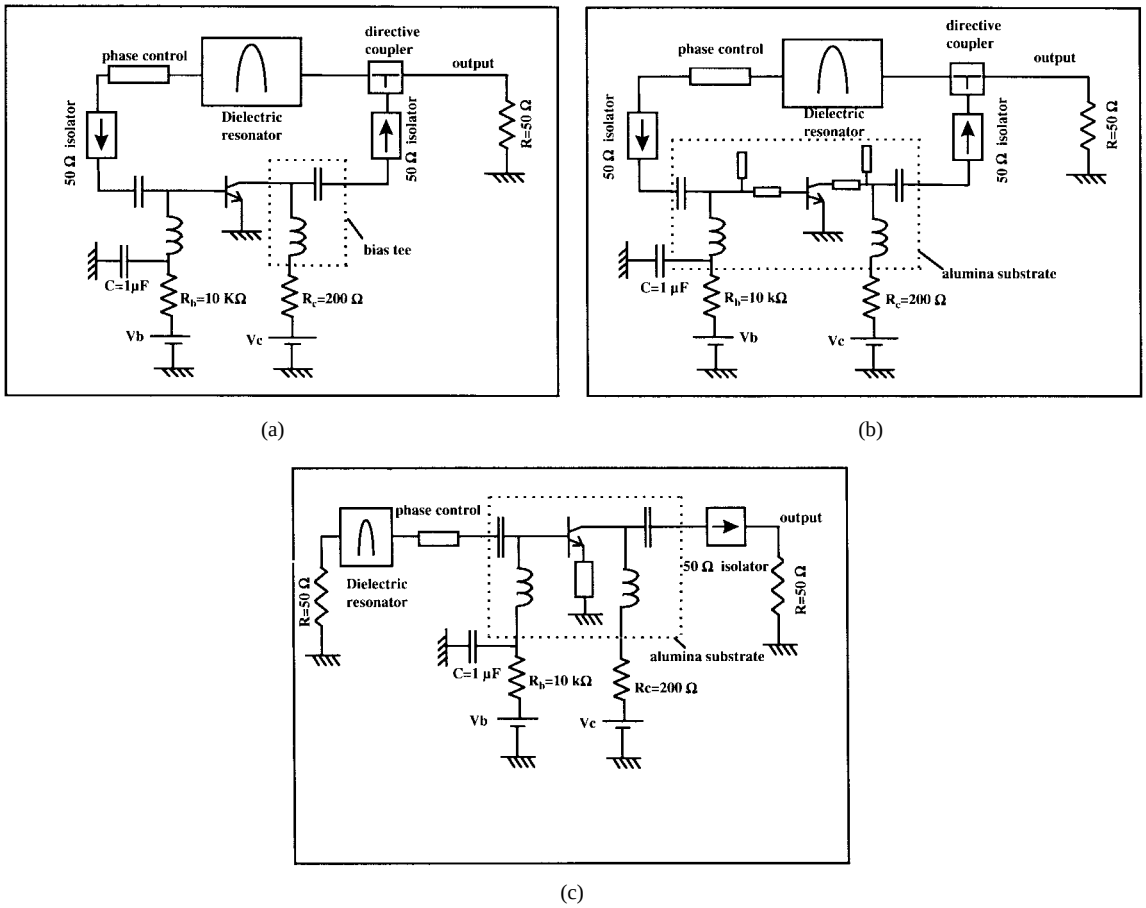

Fig. 3. DRO's circuits used for the phase-noise simulations and the circuits design. (a) Parallel feedback (transistor maintained on 50 Ω). (b) Parallel feedback (transistor matched for high gain). (c) Serial feedback.

the emitter resistance has also been proposed [13], but it results in a decrease of the transistor gain, which is not high enough at microwave frequencies on our BJT devices. Taking into account these LF conditions, we have performed different simulations with different high-frequency conditions (impedance, topology, etc.) in order to find a low phase-noise oscillator configuration. A problem appears when the high capacitance value on the base (which filters the current noise) is taken into account in the analysis. Of course, this capacitance has no effect on a pushing-type analysis. To circumvent the difficulty, we have used an artificial noise source calculated in such a way that this source creates, on the $V_{\rm be}$ control voltage, the same noise level that has been measured at low frequencies using a low dc (or LF) input impedance. This method works, provided that the base shunt capacitance can be considered as a short circuit at the noise frequencies, which is generally true for a few tens of microfarad capacitance and frequencies above 100 Hz [11].

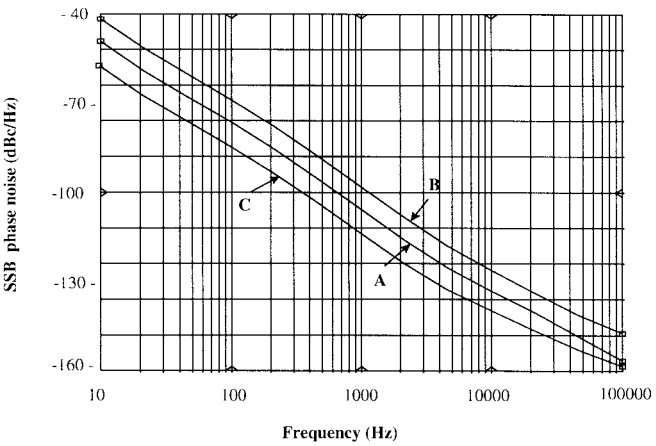

Fig. 4. Simulated phase noise with the three configurations ($f_0 = 4$ GHz, $Q_L = 1500$ $[A]$, $Q_L = 3800[B]$, $Q_L = 3000$ $[C]$).

IV. Phase-Noise-Simulation Results

In this section, the phase-noise-simulation results obtained on different oscillator configurations are described. The nonlinear transistor model is the spice equivalent circuit of the HP-MDS software. We have first investigated a parallel-feedback oscillator where the active device is maintained between the 50-Ω isolators. This topology allowed us to check the validity of the phase-noise simulation method. In Fig. 2, the simulation and measurement results obtained on a 4-GHz oscillator, using a TM-mode cavity in the feedback with a loaded Q of 160, are reported. The phase-noise characterization has been performed with a delay-line discriminator featuring a noise-floor of -125 dBc/Hz at 10-kHz offset frequency (4 GHz). A very good agreement is found between theory ad experiment, as it is shown in Fig. 2, but is has to be mentioned that, in this case, the input LF noise was measured directly on this oscillator. However, this result validates the simulation approach and the oscillator modeling.

In a second step, we have worked toward an optimization of the phase noise. The classical approach for parallel-feedback DRO's consists of minimizing the dielectric-resonator coupling in order to obtain high Q-values. The relation between the phase noise and

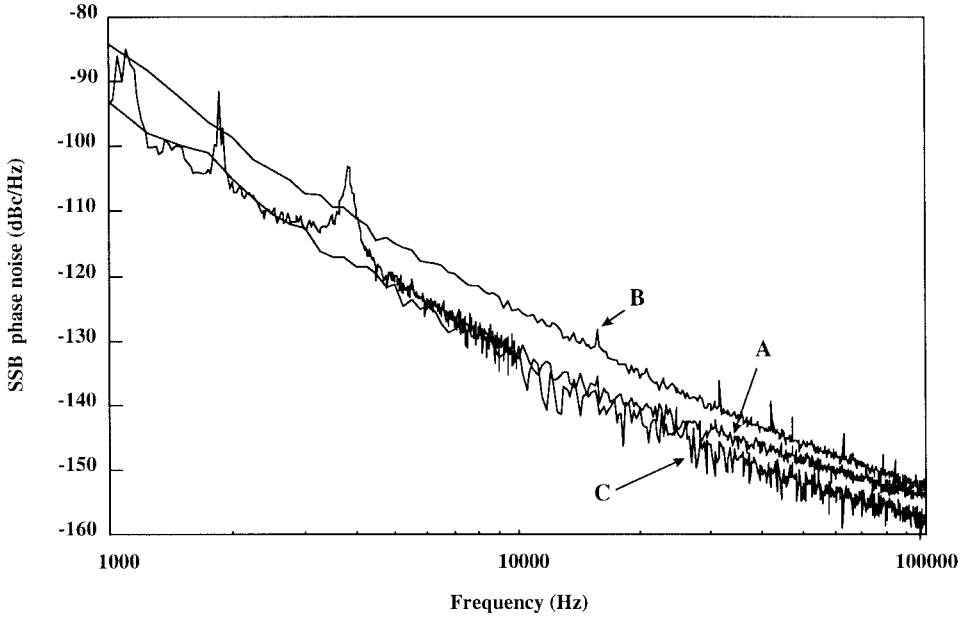

Fig. 5. Measured phase noise with the three configurations ($f_0 = 4$ GHz).

Q-factor is given by [11], [14]

$$L(f) = 20\log\frac{f_o \cdot \Delta\varphi_T}{2\sqrt{2}\cdot Q_L \cdot f} \tag{3}$$

where

- $\Delta\varphi_T$ residual phase fluctuation of the active device (rad/$\sqrt{\ }$ Hz);
- f_o oscillation frequency;
- Q_L resonator loaded Q-factor;
- f noise offset frequency.

It is obvious that increasing Q_L will reduce the phase noise, but only if $\Delta\varphi_T$ is held constant. We will see that this is not always true.

Three topologies have been investigated (see Fig. 3):

- $[A]$ parallel-feedback oscillator where the transistor is maintained between two 50-Ω isolators;
- $[B]$ parallel-feedback oscillator using a transistor matched for high gain (reference impedance $= 50\ \Omega$);
- $[C]$ serial-feedback oscillator in which the transistor is considered as a negative resistance.

Fig. 4 presents the simulation results obtained in the three configurations ($[A]$, $[B]$, and $[C]$). Curve $[A]$ corresponds to an oscillator stabilized on a resonator with a loaded Q-factor of 1500 and 2-dB losses. Indeed, the coupling level is determined by the low transistor-gain value onto 50-Ω loads. The observed phase-noise magnitude (-133 dBc/Hz at 10-kHz offset frequency) is consistent with the Q-factor ratio when compared to the results of Fig. 2. Curve $[B]$ corresponds to an oscillator which uses the same resonator, but with a coupling factor much lower, thanks to the small-signal-gain match that has been realized. The resulting loaded Q-factor is 3800, with 5.5-dB losses. The phase noise is surprisingly higher than in the first case (-127 dBc/Hz at 10 kHz) and this demonstrates that an oscillator design must not be based only on the Q-factor value: the increase of the open-loop gain also increases the open-loop phase fluctuations.

A tradeoff between high gain and low phase noise is achieved through a serial-feedback configuration. This topology allows simulated phase-noise levels below -140 dBc/Hz at 10-kHz offset frequency to be reached with a loaded Q-factor of 3000 (see Fig. 4, curve $[C]$).

In order to check the validity of these results, we have realized these three oscillators, either by using discrete elements (parallel-feedback $[A]$) or an hybrid technology on alumina substrate (parallel-feedback $[B]$ and serial-feedback $[C]$). In both cases, a line stretcher has been used in order to find the optimum phase condition for an oscillation at the resonator center frequency.

V. Measurement Results

The measurements have been performed with a frequency discriminator based on a high Q resonator of the same type of the one used in the oscillators. We use a two-mixer technique, which allows one to reach a phase-noise floor lower than -135 dBc/Hz at 10 kHz or -160 dBc/Hz at 100-kHz offset frequency. A Faraday's shielding reduces the electrical LF perturbations that are one of the major problems in the characterization of this type of oscillators. However, for parallel-feedback oscillators, the plot has been restricted to the 1–100-kHz range because of the presents (at lower frequencies) of parasitic signals coming from an amplifier used to obtain a high enough level on the mixers inputs (no such problems occurred with the serial-feedback oscillator, thanks to a sufficient output level). The phase-noise measurements are depicted in Fig. 5. It is important to note that there is a good correlation between simulations and measurements for parallel feedback ($[A]$ and $[B]$). In the third topology $[C]$, the oscillator was found to be much more unstable than the parallel-feedback oscillators with the occurrence of chaotic regimes while tuning the bias conditions or the LF loads (capacitance). This problem has been solved using an active biasing circuit, which has allowed one to minimize the collector-current variations and to stabilize the circuit quiescent point. The measured phase noise is close to the simulated one for frequencies higher than 1-kHz offset from the carrier. For frequencies lower than this offset, the observed phase-noise increase is suspected to be partly due to parasitics signals induced by mechanical vibrations.

Finally, the key idea that is revealed by this study is that a configuration with a maximum gain and a maximum resonator decoupling is not suitable for low phase-noise operation, in spite of a high loaded Q. The same effect has been observed in FET oscillators through residual phase-noise measurements of FET amplifiers [15]. Some authors [16] already recommended a resonator coupling such that $Q_L = Q_o/2$ as an optimum coupling coefficient. The theoretical

background of [16] is very different from out approach, which concentrates on the additive phase fluctuations of the transistor (3); however, the final result is the same and can be stated as follows: increasing the loaded Q above $Q_o/2$ is not necessary, and a compromise between gain and frequency sensitivity to voltage fluctuations seems to be indicated more).

VI. Conclusion

This paper reports on the nonlinear simulation, realization, and measurement of various types of BJT DRO's. In the parallel-feedback designs, the lower phase-noise level has been obtained with the transistor loaded onto 50 Ω, both through simulation and measurement. The simulation of a serial-feedback oscillator demonstrates great capabilities compared to the parallel-feedback case. However, this has not been fully confirmed by the experiment, probably due to instability problems. These problems are quite common in high-frequency bipolar devices, particularly on silicon devices which feature high-gain values at relatively low frequencies, and are hardly detected by simulation. Today, this study is extended to Si/SiGe HBT oscillators, which features almost the same noise performances, but with higher capabilities in the operation frequency.

References

[1] V. Rizzoli, F. Mastri, and D. Masotti, "General noise analysis of non linear microwave circuits by the piecewise harmonic-balance technique," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 807–819, May 1994.

[2] J. J. Siweris and B. Schieck, "Analysis of noise upconversion in microwave FET oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 233–242, Mar. 1985.

[3] O. Llopis, J. Verdier, R. Plana, and J. Graffeuil, "Low frequency noise in FET's devices operated under nonlinear conditions—consequences on oscillator phase noise," in *Proc. European Microwave Conf.*, Bologna, Italy, 1995, pp. 285–289.

[4] M. Prigent and J. Obregon, "Outil de CAO Pour la Simulation Non Linéaire des Spectres de Bruit de Phase et D'amplitude des Oscillateurs à Transistors à Effet de Champs," *Ann. Telecommun.*, vol. 44, no. 11–12., pp. 656–671, 1989.

[5] J. M. Paillot, J. C. Nallatamby, M. Hessane, R. Quere, M. Prigent, and J. Rousset, "A general program for steady state, stability, and FM noise analysis of microwave oscillators," in *IEEE MTT Symp. Dig.*, Dallas, TX, 1990, pp. 1287–1290.

[6] R. G. Rogers, *Low Phase Noise Microwave Oscillator Design.* Norwood, MA: Artech House, 1991.

[7] B. van Haaren, M. Regis, O. Llopsis, L. Escotte, A. Gruhle, C. Mähner, R. Plana, and J. Graffeuil, "Low frequency noise properties of SiGe HBT's and application to ultra low phase noise oscillators," *IEEE Trans. Microwave Theory Tech.*, to be published.

[8] O. Llopis, Jacques Verdier, R. Plana, and J. Graffeuil, "The active characterization and modeling problem in low phase noise microwave oscillator design," *Ann. Telecommun.*, vol. 51, no. 7–8, pp. 344–350, 1996.

[9] E. C. Niehenke and P. A. Green, "A low-noise L band dielectric resonator stabilized microstrip oscillator," in *IEEE MTT Symp. Dig.*, Las Vegas, NV, 1987, pp. 193–196.

[10] H. Rodin, C. Y. Su, and C. Stolte, "A study of the relation between device low frequency noise and oscillator phase noise for GaAs MESFET's," in *IEEE MTT Dig.*, San Francisco, CA, 1984, pp. 267–269.

[11] O. Llopis, J. M. Dienot, J. Verdier, R. Plana, M. Gayral, and J. Graffeuil, "Analytical investigation of frequency sensitivity in microwave oscillators: Application to the computation of phase noise in dielectric resonator oscillators," *Ann. Telecommun.*, vol. 51, no. 3–4, pp. 121–129, 1996.

[12] M. N. Tutt, D. Pavlidis, A. Khatibzadeh, and B. Bayraktaroglu, "The role of baseband noise and its upconversion in HBT oscillator phase noise," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1461–1471, July 1995.

[13] F. L. Walls, E. S. Ferre-Pikal, and S. R. Hefferts, "Origin of $1/f$ PM and AM noise in bipolar junction transistor amplifiers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 44, no. 2, pp. 326–334, Mar. 1997.

[14] T. E. Parker, "Characteristics and sources of phase noise in stable oscillators," presented at the IEEE Frequency Control Symp., 1987.

[15] O. Llopis, J. Verdier, M. Regis, R. Plana, M. Gayral, and J. Graffeuil, "Correlation between microwave transistors low frequency noise, amplifiers residual phase noise, and oscillators phase noise—consequences on oscillator phase noise modeling," in *NATO-ARW.* Norwell, MA: Kluwer, 1996.

[16] J. K. A. Everard, "Low noise oscillators," in *IEEE MTT Symp. Dig.*, Albuquerque, NM, pp. 1077–1080.